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**In the Claims:**

1-22 (cancelled)

23. (new) A device comprising:

a plurality of processing means connected to a buffer means which is connected to communication bus which is connected to a plurality of remote devices where said remote device will have a default address when added to the communication bus, and said processing means issues a general config address command to a plurality of remote devices through the communication bus, which will put the remote devices into a wait status, and when the processing means issues a general command address to all the remote devices on the communication bus the remote devices will act as being addressed with their address.

24. (new) The device according to claim 23 wherein the buffer means is a IIC buffer with a high impedance disconnection circuit.

25. (new) The device according to claim 23 wherein a IIC protocal is used.

26. (new) The device according to claim 23 wherein the buffer means is an IIC buffer and the buffer is connected by a high impedance disconnection circuit to the processing means, and which said disconnection circuit will disconnect said IIC buffer based on a BUS_En signal.

27. (new) The device according to claim 23 wherein said remote device is connected to a peripheral device.

28. (new) The device according to claim 23 wherein said remote device is a microcontroller.

29. (new) The device according to claim 23 wherein said remote device is comprised of a microcontroller, RAM memory, ROM memory, a non-volatile memory, an IIC communication port with SCL and SDA lines, an I/O port for interconnection with a peripheral device, a relay port with COM, NC and NO contacts, an ADC converter for analogical voltage readings, a timer WDT, a POWER conditioning system, and an information processing means.

30. (new) The device according to claim 23 wherein the communication bus is connected to the remote device through a high impedance disconnection means.

31. The device according to claim 23 wherein the buffer is a bi-directional IIC buffer which amplifies the signal on the communication bus.

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32. (new) The device according to claim 23 where an extender is used to allow remote devices to be connected over the IIC bus.

33. (new) The device according to claim 23 wherein said the high impedance switch makes it possible to use of two networks of different speeds connected to the same master.

34. (new) A process for connecting a serial communication network to remote devices comprising the steps of:

Connecting a plurality of processing means to a buffer means, connecting the buffer means to a communication bus and connecting the communication bus to a plurality of remote devices having a default address for said remote device, having the processing means issue a general config address command to a plurality of remote devices through the communication bus, putting the remote devices into a wait status, and having the processing unit issue a general command address all the remote devices and having the remote devices acting as being addressed with their address.

35. (new) The process according to claim 34 wherein the buffer means is an IIC buffer with a high impedance disconnection circuit.

36. (new) The process according to claim 34 wherein a IIC protocol is used.

37. (new) The process according to claim 34 wherein the buffer means is an IIC buffer and includes connecting the buffer with a high impedance disconnection circuit to the processing means, and having said disconnection circuit disconnecting said IIC buffer based on a BUS_En signal.

38. (new) The process according to claim 34 which includes the step of connecting said remote device is connected to a peripheral device.

39. (new) The process according to claim 34 wherein said remote device is a microcontroller.

40. (new) The process according to claim 34 wherein said remote device is comprised of a microcontroller, RAM memory, ROM memory, a non-volatile memory, an IIC communication port with SCL and SDA lines, an I/O port for interconnection with a peripheral device, a relay port with COM, NC and NO contacts, an ADC converter for analogical voltage readings, a timer WDT, a POWER conditioning system, and an information processing means.

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41. (new) The process according to claim 34 which includes the step of connecting  the communication bus to the remote device through a high impedance disconnection.

42. (new) The process according to claim 34 which adds the step of amplifying the signal on the communication bus using a bi-directional IIC buffer.

43. (new)  The process according to claim 34 which includes the steps of having an extender is used to allow remote devices to be connected over the IIC bus.

44. (new) The device according to claim 34 wherein said the high impedance switch makes it possible to use of two networks of different speeds connected to the same master.

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